What is claimed is:

1. A method to improve solder bump reliability for interconnection of flip chip devices, comprising the steps of:

providing a substrate, at least one a contact pad having been provided over the surface of said substrate, a layer of passivation having been deposited over the surface of said substrate, said layer of passivation having been patterned and etched, exposing the surface of said at least one contact pad, a layer of Under Ball Metal (UBM) having been deposited over the surface of said layer of passivation including the exposed surface of said at least one contact pad;

creating at least one T-shaped layer of solder compound over the surface of said layer of UBM in at least one opening created in a layer of patterning material, said at least one T-shaped layer of solder compound being aligned with said at least one contact pad having been provided over the surface of said substrate;

removing said layer of patterning material, leaving in place said at least one T-shaped layer of solder compound, exposing the surface of said patterned layers UBM;

etching said exposed layer of UBM using said at least one T-shaped layer of solder compound as a mask; and

reflowing the surface of said solder compound, creating said solder bump.

2. The method of claim 1, said layer of patterning material comprising photoresist.

3. The method of claim 1, said layer of Under Bump Metallurgy comprising a layer of chromium followed by a layer of copper followed by a layer of gold.

4. The method of claim 1, said layer of Under Bump Metallurgy comprising a plurality of sub-layers of different metallic composition.

5. The method of claim 1, said passivation layer deposited over the surface of said semiconductor surface comprising a plurality of passivation layers.

6. The method of claim 5, at least one of said plurality of passivation layers being selected from the group consisting of PE $Si_3N_4$ and $SiO_2$ and a photosensitive polyimide and phosphorous doped silicon dioxide and titanium nitride.

7. The method of claim 1, said contact pad on said semiconductor surface being electrically connected with a semiconductor device

with at least one conductive line of interconnect or with at least one conductive contact point.

8. The method of claim 1, said contact pad on said semiconductor substrate further being expanded to include a contact pad that is formed on a surface that is selected from the group of surfaces consisting of printed circuit boards and flex circuits and a metallized or glass substrate and a semiconductor device mounting support.

9. The method of claim 1 with an additional step of applying a solder flux to the surface of said solder compound, said additional step to be performed prior to said reflowing the surface of said solder compound.

10. The method of claim 1, said step of patterning and etching said layer of UBM being further expanded, leaving said layer of UBM in place above and extending from above said at least one contact pad by a measurable amount, simultaneously creating conductive interconnect lines on the surface of said layer of passivation, said conductive interconnect lines making contact with at least one contact pad on said semiconductor substrate by creating openings in said layer of passivation that align with at least one contact pad on said semiconductor substrate.

11. The method of claim 1 wherein said creating at least one T-shaped layer of solder compound over the surface of said layer of UBM in at least one opening created in a layer of patterning material comprises the steps of:

depositing a layer of patterning material over the surface of said layer of UBM; and

patterning and developing said layer of patterning material using a grey-tone mask, creating at least one opening having a T-shape through said layer of patterning material, exposing the surface of said layer of UBM.

12. The method of claim 11 wherein said grey-tone mask comprises:

at least one pattern of two concentric patterns of opaque material;

a first pattern of said two concentric patterns of opaque material being a pattern that surrounds said second pattern having a thickness;

a second pattern of said two concentric patterns surrounding a transparent surface area of said grey-tone mask, said transparent surface area being aligned with said at least one contact pad provided on the surface of said substrate; and

said first pattern having a thickness that is larger than a thickness of said first pattern by a measurable amount.

13. The method of claim 11, with an additional step of performing an in-situ sputter clean of inside surfaces of said at least one opening having a T-shape created through said layer of patterning material and said exposed surface of said layer of UBM.

14. The method of claim 13, with an additional step of depositing a seed layer over inside surfaces of said at least one opening having a T-shape created through said layer of patterning material and said exposed surface of said layer of UBM.

15. A method to improve solder bump reliability for interconnection of flip chip devices, comprising the steps of:

providing a substrate, active semiconductor devices having been created in or on the surface of said substrate;

creating at least one a contact pad over the surface of said substrate;

depositing a layer of passivation having over the surface of said substrate, including the surface of said at least one contact pad;

patterning and etching said layer of passivation, exposing the surface of said at least one contact pad;

depositing a layer of Under Ball Metal (UBM) over the surface of said layer of passivation, including the exposed surface of said at least one contact pad;

depositing a layer of exposure sensitive material over the surface of said layer of UBM;

patterning and etching said layer of exposure sensitive material, creating at least one opening having a T-shaped cross section through said exposure sensitive material, said at least one opening being aligned with said at least one contact pad created over the surface of said substrate;

filling said at least one opening created through said exposure sensitive material with a solder compound;

removing said exposure sensitive material from the surface of said layer of UBM, leaving in place at least one T-shaped layer of solder compound, exposing the surface of said layer of UBM;

etching said layer of UBM, using said at least one T-shaped layer of solder compound as a mask; and

reflowing said at least one T-shaped layer of solder compound.

16. The method of claim 15, said layer of exposure sensitive material comprising photoresist.

17. The method of claim 15, said layer of Under Bump Metallurgy comprising a layer of chromium followed by a layer of copper followed by a layer of gold.

18. The method of claim 15, said layer of Under Bump Metallurgy comprising a plurality of sub-layers of different metallic composition.

19. The method of claim 15, said passivation layer deposited over the surface of said semiconductor surface comprising a plurality of passivation layers.

20. The method of claim 19, at least one of said plurality of passivation layers being selected from the group consisting of PE $Si_3N_4$ and $SiO_2$ and a photosensitive polyimide and phosphorous doped silicon dioxide and titanium nitride.

21. The method of claim 15, said contact pad on said semiconductor surface being electrically connected with a semiconductor device with at least one conductive line of interconnect or with at least one conductive contact point.

22. The method of claim 15, said contact pad on said semiconductor substrate further being expanded to include a contact pad that is formed on a surface that is selected from the group of surfaces consisting of printed circuit boards and

flex circuits and a metallized or glass substrate and a semiconductor device mounting support.

23. The method of claim 15, with an additional step of applying a solder flux to the surface of said solder compound, said additional step to be performed prior to said reflowing the surface of said solder compound.

24. The method of claim 15, said step of patterning and etching said layer of UBM being further expanded, leaving said layer of UBM in place above and extending from above said at least one contact pad by a measurable amount, simultaneously creating conductive interconnect lines on the surface of said layer of passivation, said conductive interconnect lines making contact with at least one contact pad on said semiconductor substrate by creating openings in said layer of passivation that align with at least one contact pad on said semiconductor substrate.

25. The method of claim 15, said patterning and etching said layer of exposure sensitive material, creating at least one opening having a T-shaped cross section through said exposure sensitive material comprising the steps of:

depositing a layer of exposure sensitive material over the surface of said layer of UBM; and

patterning and developing said layer of exposure sensitive material using a grey-tone mask, creating at least one opening having a T-shape through said layer of patterning material, exposing the surface of said layer of UBM.

26. The method of claim 25 wherein said grey-tone mask comprises:

at least one pattern of two concentric patterns of opaque material;

a first pattern of said two concentric patterns of opaque material being a pattern that surrounds said second pattern having a thickness;

a second pattern of said two concentric patterns surrounding a transparent surface area of said grey-tone mask, said transparent surface area being aligned with said at least one contact pad provided on the surface of said substrate; and

said first pattern having a thickness that is larger than a thickness of said first pattern by a measurable amount.

27. The method of claim 25, with an additional step of performing an in-situ sputter clean of inside surfaces of said at least one opening having a T-shape created through said layer of patterning material and said exposed surface of said layer of UBM.

28. The method of claim 27, with an additional step of depositing a seed layer over inside surfaces of said at least one opening having a T-shape created through said layer of patterning material and said exposed surface of said layer of UBM.